

WHAT IS CLAIMED IS:

1 1. A method for determining a cracking threshold for a dielectric material on a substrate  
2 comprising the steps of:

3 forming two or more test structures on the substrate, each test structure comprising  
4 two metal structures separated by the dielectric material having a width which is different for  
5 each test structure; and

6 determining whether the dielectric material between the two metal structures for each  
7 test structure has cracked during processing, the cracking threshold being approximately  
8 equal to the largest width of dielectric material that is cracked.

1 2. The method as recited in claim 1, wherein the step of determining whether the  
2 dielectric material between the two metal structures for each test structure has cracked during  
3 processing is performed by electrically probing the two metal structures in each test structure  
4 to measure a leakage current across the width of the dielectric material for each test structure.

1 3. The method as recited in claim 1, wherein the step of determining whether the  
2 dielectric material between the two metal structures for each test structure has cracked during  
3 processing is performed by optically inspecting the width of the dielectric material for each  
4 test structure.

1 4. The method as recited in claim 1, wherein the dielectric material is a low-k dielectric  
2 material chosen from the group consisting of polyimide, silicon oxycarbide, hydrogen  
3 silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass, fluorinated  
4 aromatic ether, and inter-penetrated spin-on glass.

1 5. A test pattern for determining a cracking threshold for a dielectric material on a  
2 substrate comprising:

3 two or more test structures disposed on the substrate;

4 each test structure comprising two metal structures separated by the dielectric  
5 material having a width which is different for each test structure; and

6 wherein the cracking threshold is approximately equal to the largest width of  
7 dielectric material that is cracked after processing.

1 6. The test pattern as recited in claim 5, wherein the dielectric material is a low-k  
2 dielectric material chosen from the group consisting of polyimide, silicon oxycarbide,  
3 hydrogen silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass,  
4 fluorinated aromatic ether, and inter-penetrated spin-on glass.

1 7. The test pattern as recited in claim 5, wherein the two metal structures are copper.

1 8. The test pattern as recited in claim 5, further comprising a barrier layer surrounding  
2 each metal structure.

1 9. The test pattern as recited in claim 5, wherein each metal structure comprises a  
2 damascene structure containing a metal.

1 10. The test pattern as recited in claim 5, wherein the test structures are disposed on more  
2 than one layer of a silicon-on-insulator structure.

1 11. The test pattern as recited in claim 5, wherein the width is within a range of 0.05 and  
2 1.0  $\mu\text{m}$ .

1 12. The test pattern as recited in claim 5, wherein the width of the dielectric material for  
2 the two or more test structures differs by approximately 0.05  $\mu\text{m}$ .

1 13. The test pattern as recited in claim 5, further comprising a sealing ring disposed  
2 around each test structure.

1 14. The test pattern as recited in claim 13, wherein the separation between the sealing  
2 ring and the two metal structures exceeds the width.

1 15. The test pattern as recited in claim 5, wherein each test structure comprises:  
2 two or more test substructures; and  
3 each test substructure includes two metal structures having a first width which is  
4 different for each test substructure, the two metal structures separated by the dielectric  
5 material having a second width which is substantially constant for each test substructure and  
6 different for each test structure.

1 16. The test pattern as recited in claim 15, wherein the first width is selected from a range  
2 of 1 to 30  $\mu\text{m}$  and the second width is selected from a range of 0.05 to 1.0  $\mu\text{m}$ .

1 17. The test pattern as recited in claim 15, wherein the two or more test substructures are  
2 arranged in a pyramid pattern.

1 18. The test pattern as recited in claim 15, wherein:  
2 the first width for the first test substructure, second test substructure, third test  
3 substructure, fourth test substructure and fifth test substructure is approximately 3, 5, 10, 15  
4 and 20  $\mu\text{m}$ , respectively; and

5           the second width for the first test structure, second test structure, third test structure;  
6   fourth test structure, fifth test structure, sixth test structure, seventh test structure, eighth test  
7   structure, ninth test structure, tenth test structure, eleventh test structure and twelfth test  
8   structure is approximately 0.1, 0.2, 0.25, 0.3, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, and 0.8  $\mu\text{m}$ ,  
9   respectively.

1 19. A test pattern comprising:  
2 two or more test structures disposed on a substrate;  
3 each test structure includes two or more test substructures; and  
4 each test substructure comprising a sealing ring, two metal structures having a first  
5 width which is different for each test substructure, and a dielectric material disposed between  
6 each metal structure and the sealing ring and between the two metal structures, the dielectric  
7 material between the two metal structures having a second width which is substantially  
8 constant for each test substructure and different for each test structure.

1 20. The test pattern as recited in claim 19, wherein the dielectric material is a low-k  
2 dielectric material chosen from the group consisting of polyimide, silicon oxycarbide,  
3 hydrogen silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass,  
4 fluorinated aromatic ether, and inter-penetrated spin-on glass.

1 21. The test pattern as recited in claim 19, wherein the two metal structures are copper.

1 22. The test pattern as recited in claim 19, further comprising a barrier layer surrounding  
2 each metal structure.

1 23. The test pattern as recited in claim 19, wherein each metal structure comprises a  
2 damascene structure containing a metal.

1 24. The test pattern as recited in claim 19, wherein the test structures are disposed on  
2 more than one layer of a silicon-on-insulator structure.

1 25. The test pattern as recited in claim 19, wherein the first width is selected from a range  
2 of 1 to 30  $\mu\text{m}$  and the second width is selected from a range of 0.05 to 1.0  $\mu\text{m}$ .

1 26. The test pattern as recited in claim 19, wherein the second width of the dielectric  
2 material for the two or more test structures differs by approximately 0.05  $\mu\text{m}$ .

1 27. The test pattern as recited in claim 19, wherein the separation between the sealing  
2 ring and the two metal structures exceeds the second width.

1 28. The test pattern as recited in claim 19, wherein the two or more test substructures are  
2 arranged in a pyramid pattern.

1 29. The test pattern as recited in claim 19, wherein:  
2 the first width for the first test substructure, second test substructure, third test  
3 substructure, fourth test substructure and fifth test substructure is approximately 3, 5, 10, 15  
4 and 20  $\mu\text{m}$ , respectively; and  
5 the second width for the first test structure, second test structure, third test structure,  
6 fourth test structure, fifth test structure, sixth test structure, seventh test structure, eighth test  
7 structure, ninth test structure, tenth test structure, eleventh test structure and twelfth test  
8 structure is approximately 0.1, 0.2, 0.25, 0.3, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, and 0.8  $\mu\text{m}$ ,  
9 respectively.